400G QSFP-DD Active Optical Cables Specification

Features:

- Hot Pluggable QSFP-DD Cable End
- Supports 425Gb/s aggregate bit rate
- Low Power Dissipation, Typ. 10W Each End
- 8x50G PAM4 VCSEL/PIN photo detector
- Operating Case Temperature: 0℃~70
- Compliant to QSFP-DD Rev 4.0
- Compliant to Class 1M Laser Safety
- SFF-8636 Management Interface
- SFF-8679: General Electrical
- IEEE 802.3bs: Physical Layer Specifications and Management Parameters
- ROHS-6: Environment Safety

Applications

- Ethernet for 400GBASE-SR8

Order Information

Part Number	From Factor	Data Rate	Media	Distance① (m)	Wavelength (nm)	Voltage (V)	Temperature (℃)
AOC-QSFPDD-5M	QSFP-DD	400Gbps	MMF	5	850	3.3	0/+70
AOC-QSFPDD-10M	QSFP-DD	400Gbps	MMF	10	850	3.3	0/+70
AOC-QSFPDD-15M	QSFP-DD	400Gbps	MMF	15	850	3.3	0/+70
AOC-QSFPDD-20M	QSFP-DD	400Gbps	MMF	20	850	3.3	0/+70

① Cable length can be customized upon customer's request.

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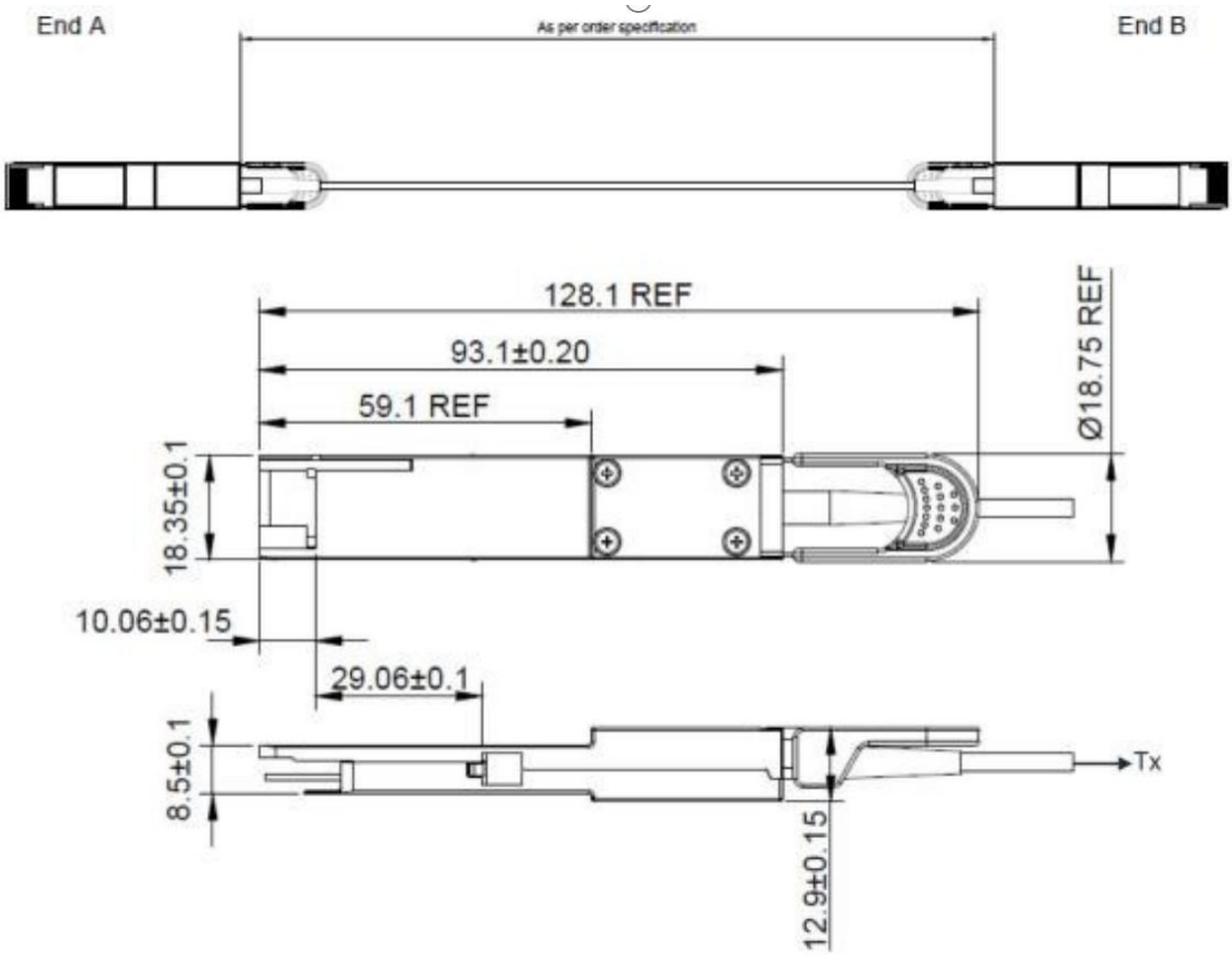
MECHANICAL SPECIFICATION

Product shall be of design, construction and physical dimensions specified on applicable product drawing.



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GENERAL PRODUCT CHARACTERISTICS

Parameter	Value	Unit	Comments
Module Form Factor	QSFP-DD	As defined by QSFF-DD Rev 3.0	Module Form Factor
Number of Lanes	8 TX and 8 RX		
Maximum Aggregate Data Rate	425	Gb/s	
Standard Cable Lengths	3, 5, 7, 10, 15, 20	meters	Other lengths may be available upon request
Protocols Supported	Ethernet		
Electrical Interface and Pin-out	76-pin edge connector		Pin-out as defined by QSFF-DD Rev 3.0
Typical Power Consumption per End	12	Watts	Varies with output voltage swing and pre-emphasis settings
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by SFF-8636

The force specification for AOC is in the list below:

Parameter	Min.	Max.	Unit.	Comments.
QSFP-DD Module Insertion		90	Newton	
QSFP-DD Module Extraction		50	Newton	
QSFP-DD Module Retention	90		Newton	
Insertion and removal cycles	50		Cycle	
Cable outer Diameter	2.9	3.0	mm	

ABSOLUTE MAXIMUM PARAMETERS

Exceeding the limits below may damage the active optical cable permanently.

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Maximum Supply Voltage	V_{cc}	-0.5		3.6	V	
Storage Temperature	T_{sto}	-40		85	℃	
Case Operating Temperature	T_{op}	0		70	℃	
Relative Humidity	RH	0		85	%	①

① No-condensing.

PARAMETERS

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Supply Voltage	V_{cc}	3.14		3.46	V	
Power Consumption	P_{Con}		10	12	W	
Bit Rate	BR		26.5625		GBd	①
Bit Error Ratio	BER	10^{-6}				②
Center wavelength	λ_c	840		860	nm	③
Beam divergence angle			23		°	
Number of Lanes		8				
Management Interface		Serial, I2C-based, maximum frequency 400 kHz				④
Logic Input Voltage High	V_{ih}	2		Vcc+0.3	V	
Logic Input Voltage Low	V_{il}	-0.3		0.8	V	

① Single lane

② PRBS13Q test pattern is used.

③ As defined by IEEE Std. 802.3bs ™/D3.5

④ As defined by SFF-8636

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transceiver Power Supply Current	I_{cc}		3100		mA	
Transceiver Power On Initialization Time	T_{init}			2000	ms	
Transmitter at TP1a						
AC common-mode output voltage(RMS)				17.5	mV	
Differential peak-to-peak output voltage (Transmitter disabled)				35	mV	
Differential peak-to-peak output voltage (Transmitter enabled)				880	mV	
Eye symmetry mask width	ESMW		0.22		UI	
Eye height, differential	EH	32			mV	
Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential termination mismatch		10			%	
Transition time (20% to 80%)	Tr, Tf	10			ps	
Receiver at TP4						
Far-end Eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential termination mismatch		10			%	
Transition time (20% to 80%)	Tr, Tf	10			ps	
DC common mode voltage		-350		2850	mV	

1. $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(Eq.1)}$$

where

f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss

2. $$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(Eq.2)}$$

where

f is the frequency in GHz,

RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

PIN DESCRIPTIONS (compliant SFF-8679)

PIN	Symbol	Description	Ref.
1	GND	Ground	①
2	TX2n	Transmitter Inverted Data Input	
3	TX2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	①
5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	①
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc RX	+3.3V Power Supply Receiver	②
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	①
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	①
17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	①
20	GND	Ground	①
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	①
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	①
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc TX	+3.3V Power supply transmitter	②
30	Vcc1	+3.3V Power supply	②
31	LPMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32	GND	Ground	①
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	①
36	TX1p	Transmitter Non-Inverted Data Input	
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	①

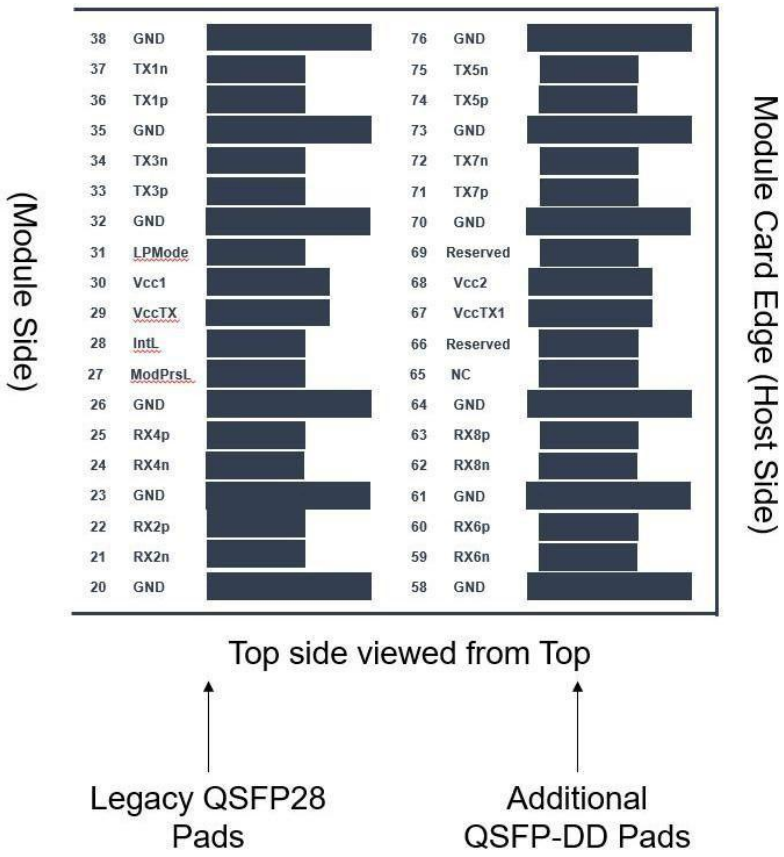
PIN	Symbol	Description	Ref.
39	GND	Ground	①
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	①
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	①
46	Reserved	For future use	③
47	VS1	Module Vendor Specific 1	③
48	3.3V Power Supply	2A	②
49	VS2	Module Vendor Specific 2	③
50	VS3	Module Vendor Specific 3	③
51	GND	Ground	①
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	①
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	①
58	GND	Ground	①
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	①
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	①
65	NC	No Connect	③
66	Reserved	For future use	③
67	VccTx1	3.3V Power Supply	②
68	Vcc2	3.3V Power Supply	②
69	Reserved	For Future Use	③
70	GND	Ground	①
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	①
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	①

① QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unlessotherwise noted. Connect these directly to the host board signal-common ground plane.

② VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc ping are each rated for a maximum current of 1000 mA.

③ All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to grounds on the host. Pad 65 (No connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10k ohms and less than 100 pF.

④ Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, the break contact with additional QSFP- DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.



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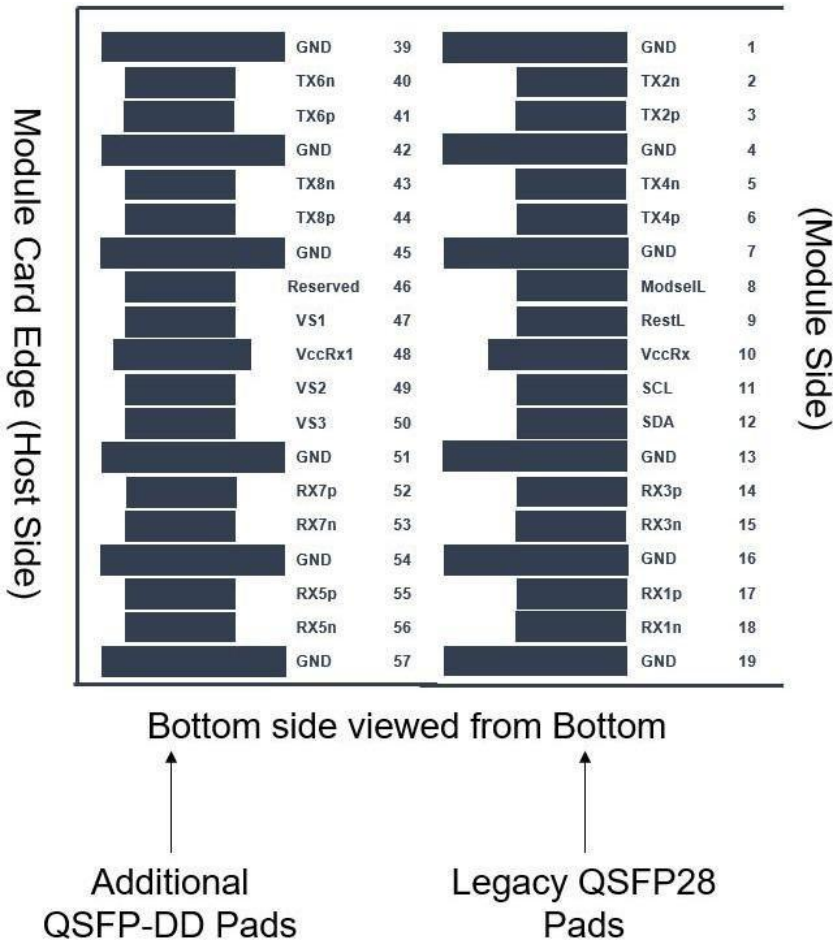
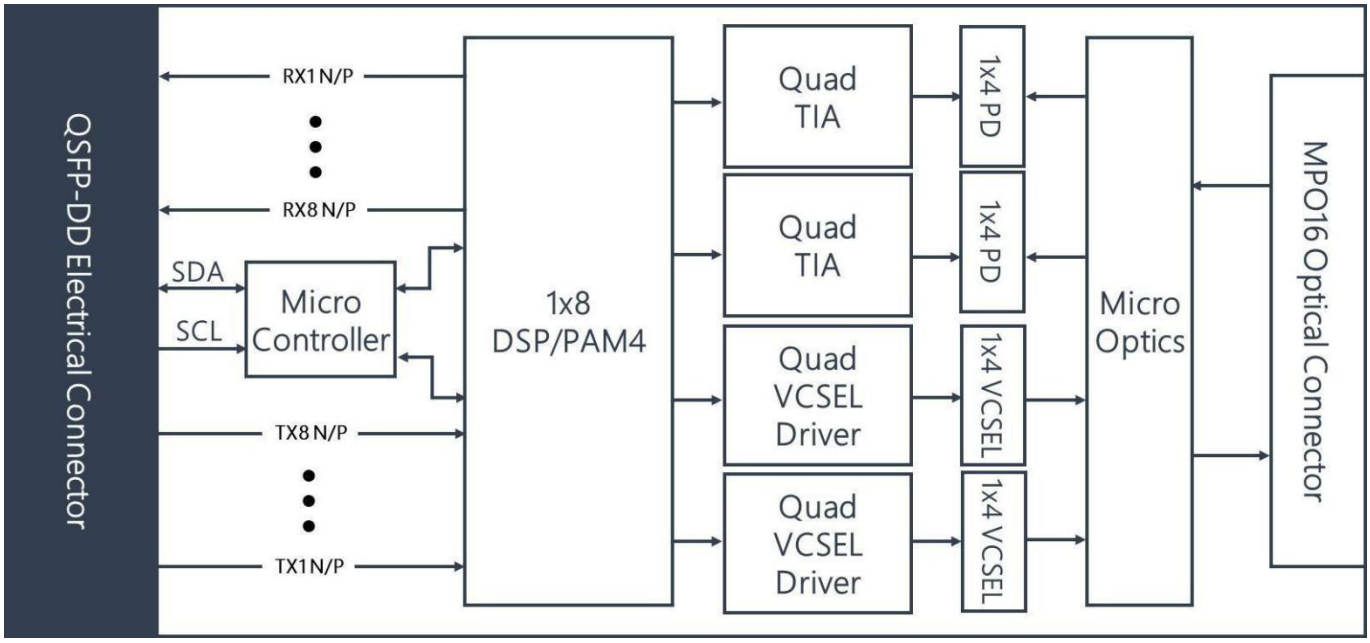


RECOMMENDED HOST BOARD SCHEMATIC



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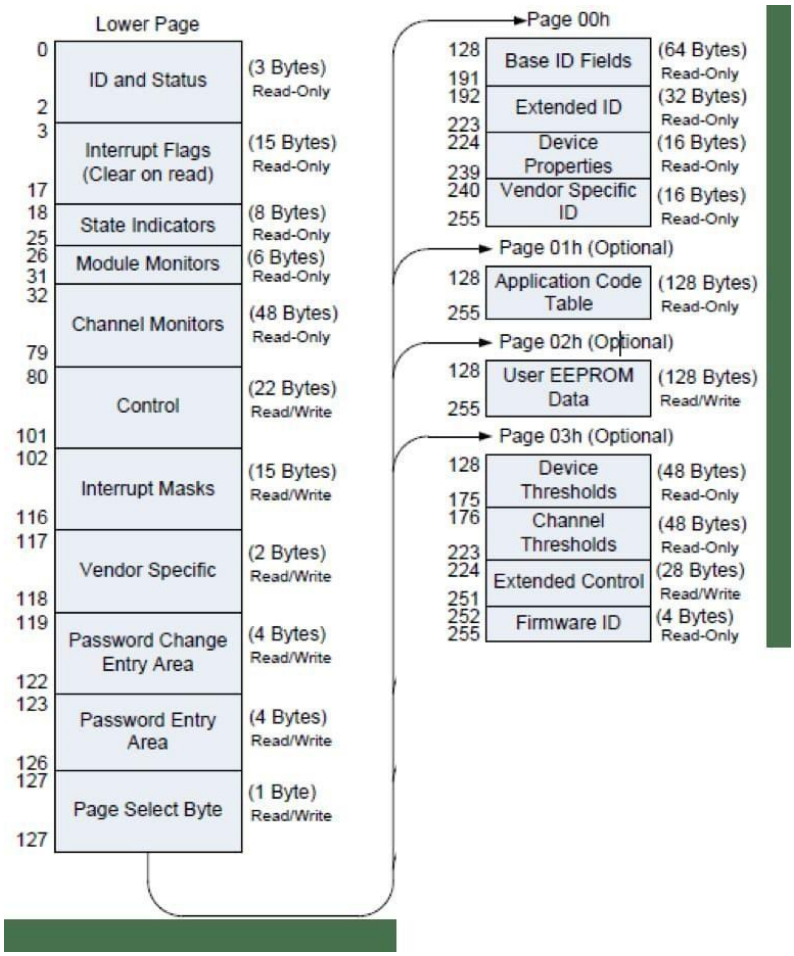
MEMORY MAP (compliant QSFP-DD Rev. 3.0)



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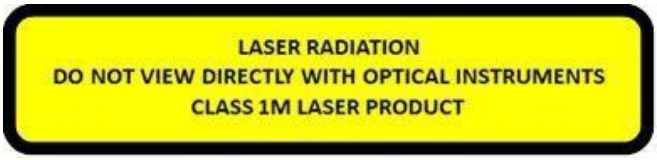
Laser Safety

All transceiver is compliance to Class 1M Laser safety products of IEC 60825-1:2007 & IEC60825-1:2014 standards. They must be operated under specified operating condition. Complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007



Caution – Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Notes:
Module circuit ground is isolated from module chassis ground within the module. GND is the symbol for signal and supply (power) common for QSFP modules.
The connector pins are each rated for a maximum current of 500mA.